Amendments to the Specification:

Please replace the Title with the following amended Title:

New Title: **PREDICATE PREDICTION IN A PROCESSOR**

B1

Please replace the second paragraph on page 8 with the following amended paragraph:

B2

- - Figure 2 is a comparator formed in accordance with an embodiment of the present invention in which the LSBs of the operand stored in register R1, 201, are compared to the LSBs of the operand stored in register R2, 202 to determine a PPV. In accordance with the embodiment of Figure 2, only the least significant five bits of the 64-bit operands are compared within comparator 203 to determine a PPC. Bits a(0) and b(0), a(1) and b(1), a(2) and b(2), a(3) and b(3), and a(4) and b(4) are compared for equality using XOR gates 210, 211, ~~223~~ 212, 213, and 214, respectively. The output of each of XOR gates 210-214 is provided to the input of NOR gate 220, the output of which is PPV. For this embodiment, a PPV of 1 indicates that the least significant five bits from the operand of register 201, a(0-a(4), are equal to the least significant five bits from the operand of register 202, b(0)-b(4). A PPV of 0 indicates that the bits are note equal to each other. - -